H3_REF_DDR3_16X2_V1_0

Layout Note

1 Stackup - Impadence -Trace Width

Stackup Control Table

---	Stackup Structure				Impedance Requirements			
Layer	Type	Thickness (mil)		Dk(with Sim Z0)	Impedance spec (Ohms)	Reference layer	Width/space (mil)	Sim Z0(Ohms)
	solder mask	0.5	SM	4.25				
1	TOP	1.6	0.3oz+plating		50±10%	2	4	52.18
					100±10%	2	3.7/8.8	98.5
	prepreg	2.9		4				
2	GND	1.2	1.0oz					
	core	27.0		4.5				
3	VCC	1.2	1.0oz					
	prepreg	2.9		4				
4	BOTTOM	1.6	0.3oz+plating		50±10%	3	4	52.18
					100±10%	3	3.7/8.8	98.5
	solder mask	0.5	SM	4.25				
	Board thickness:	39.4						

2 走线宽度

单端：外层走线线宽4mil。

差分：外层走线线宽/线距为3.7/8.8mil。

电源和地Fanout线宽≥10mil。

3 间距

单端：外层线与线的间距（Air Gap）≥8mil,内层≥8mil。

差分线：到其他网络走线间距≥15mil。

电源与地：到其他网络走线的间距≥15mil。

VREF：到其他网络走线的间距≥15mil。

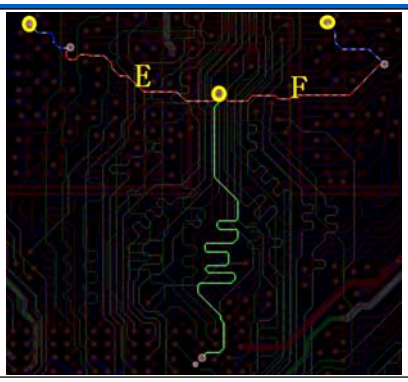
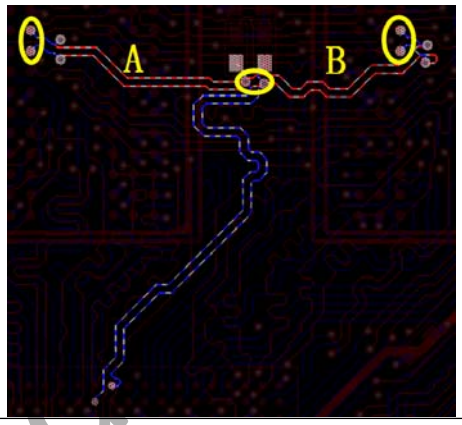
BGA区域里：线与线4mil；线与SMD PIN 4mil；线与过孔4mil。

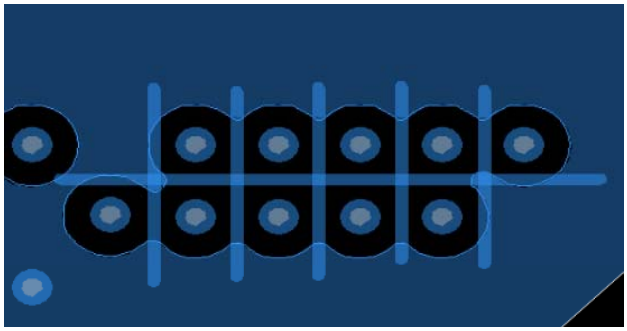
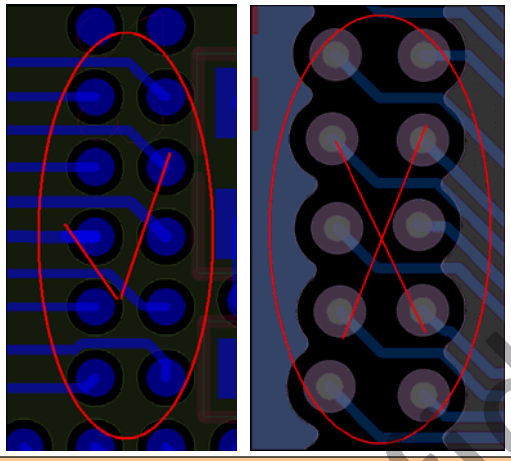
4 拓扑

DQ：单点对单点

DQS、DQSB：单点对单点

Ax、BAx、CAS、RAS、WE、CSx、ODTx、CKEx、RST：远端簇型

	对于两片颗粒： E ＜ 600mil， F ＜ 600mil， E － F ＜ +/- 50mil。 
	CK、CKB：远端簇型
	对于两片颗粒： A ＜ 600mil， B ＜ 600mil， A － B ＜ +/- 50mil。 
5	**等长**
	DQ0-7：相对于DQS0、DQSB0做等长，误差范围为≤50mil。过孔数一致。 DQ8-15：相对于DQS1、DQSB1做等长，误差范围为≤50mil。过孔数一致。 DQ16-23：相对于DQS2、DQSB2做等长，误差范围为≤50mil。过孔数一致。 DQ24-31：相对于DQS3、DQSB3做等长，误差范围为≤50mil。过孔数一致。
	DQSx、DQSBx: 相对于CK/CKB信号做等长，误差范围为≤800mil。
	Ax、BAx、CAS、RAS、WE、CSx、ODTx、CKEx： 相对于CK/CKB信号做等长，误差范围为≤600mil。
	DQSx与DQSBx等长，等长误差范围为≤10mil。 CK与CKB等长，等长误差范围为≤10mil。
	信号线做等长时要考虑过孔长度的影响
6	**电源、地平面**

	平面比较完整，调整好过孔的位置、间距，减少对电源、地平面的破坏。平面断开处用走线连接 
	电源、地平面同时也是信号的参考层要求，不能有信号线的参考层被割断的现象 
7	**滤波电容：**
	对于单面布局：尽量靠近电源PIN放置，每个电容至少各一个电源过孔和地过孔。
	对于双面布局：最好能放置在电源管脚下方的PCB背面，每个电容至少各一个电源过孔和地过孔。不同容值的电容均匀分布。

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